

REMARKS

Favorable reconsideration of this application is requested in view of the foregoing amendments and the following remarks. Claims 30-61 are pending in this application. Claims 1-12 and 27-28 are canceled without prejudice or disclaimer. Claims 13-26 and 29 were previously canceled without prejudice or disclaimer. Claims 30-61 are newly presented.

Support for new claims 30-42 is found in claims 25-26 and 29 as originally filed. It is noted that claims 25-26 and 29 were non-elected in the parent application (i.e., U.S. Ser. No. 09/653,788). Support for new claims 32-35, 38-41, 43-50, 53-56 and 58-61 is found in the embodiment depicted in figure 5, (please see elements 70, 64, 58, 54 and 55) and the associated descriptions thereof as originally filed. Support for new claims 51-61 is found in the embodiment depicted in figures 3 and 7, (please see the three the input frequencies) and the associated descriptions thereof as originally filed. Support for the recitation of the phrase multiplier phase detector is found in the paragraph bridging pages 19-20 (especially table 1); lines 11-13, page 20; and lines 15-17, page 21 of this application as originally filed. In more detail, it is well known to those of skill in the art of phase detection that analog multipliers, balanced mixers and digital XOR gates are all similar in function and performance.

The title is amended to more concisely name the claimed invention. The abstract is amended to more accurately summarize the claimed invention. The specification is amended as required by the Examiner to more clearly describe the invention.

Applicant submits herewith one copy of eight sheet(s) of replacement drawings. Applicant requests that the Examiner approve the substitute drawings. Marked-up versions of the substitute sheet(s) of drawings are attached hereto with the change(s) shown with red ink

markings. Support for the depiction of detail number 66 in figure 5 is found at line 15 of page 21 of this application as originally filed. Support for the depiction of detail number 86 in figure 5 is found at line 10 of page 22 of this application as originally filed.

At page 2 of the Office Action, the disclosure is objected to. Page 16 of the disclosure is amended as required by the Examiner.

Accordingly, withdrawal of this objection is respectfully requested.

Claims 1-5 and 9-12 were rejected under 35 USC 102(b) as anticipated by DaSilva (i.e., U.S. Patent No. 5,105,168). Claims 1-5 and 9-12 are cancelled without prejudice or disclaimer.

To expedite the prosecution of this application, Applicant provides the following remarks regarding the DaSilva reference with respect to the presently pending claims 30-61.

DaSilva teaches a vector locked loop having a topology somewhat similar to two cross coupled phase locked loops, but wherein both magnitude and phase are used as feedback signals. The output signal of DaSilva is generated by combining the outputs of two VCOs in a combiner network. This output signal is fed back to the input, where phase and magnitude detectors are used to generate error signals. These error signals are processed by DaSilva to yield control signals for controlling the frequencies of the two VCOs. DaSilva never discloses, mentions, suggest or claims any plurality of phase detectors, much less a plurality of phase detectors cooperatively controlling a plurality of VCOs.

DaSilva only cites a specific configuration which employs *pairs* of VCOs which both operate at similar carrier frequencies (separated only by the modulation frequencies. In DaSilva the two VCOs are combined to produce the single composite output signal.

DaSilva never even mentions the topic of synchronization. DaSilva teaches a phase-locked signal generator that produces an amplitude/phase-modulated signal which closely emulates an input signal in both amplitude and phase.

The amplitude detector of DaSilva (his 38) has nothing to do with signal timing (phase), only its magnitude. Very clearly, each VCO in DaSilva has only one timing (phase) error signal [signal 42 applied through difference block 40 and filter 52 into VCO 1 (12), which is precisely the same signal as 58 [applied through summer block 54 and filter 62 into VCO 2 (14)]. Thus, in DaSilva, both VCOs are each fed a **single** timing signal (16 and 18 respectively).

With regard to claims 47-55, DaSilva at no time discloses or suggests cross-coupling more than two VCOs, whereas this application as originally filed discloses methods of interlocking an arbitrarily large number of diverse-frequency VCOs, so long as their frequencies are rationally related (either multiplied or divided by integer ratios).

With regard to claims 31, 35 and 51-61, the "reference" (Input) of DaSilva can only be at the desired output frequency, except in the frequency-offset case with the mixer (please see DaSilva's figure 5).

With regard to claims 32-35, 38-41, 43-50, 53-56 and 58-61, DaSilva does not disclose or suggest a phase-frequency detector, much less a composite or digital phase-frequency detector. Specifically, DaSilva's description of his figure 3 is limited to an analog difference circuit immediately following the phase detector (i.e., the loop of DaSilva as shown and described is totally analog.

Accordingly, withdrawal of this rejection is respectfully requested.

Claims 7 and 27-28 were rejected under 35 USC 103 as obvious over DaSilva in view of Lee (i.e., U.S. Patent No. 5,568,078). Claims 7 and 27-28 are cancelled without prejudice or disclaimer.

To expedite the prosecution of this application, Applicant provides the following remarks regarding the Lee reference with respect to the presently pending claims 30-61.

The teachings of the Lee reference are directed to dealing with duty cycle restrictions of phase detectors. Lee teaches duty cycle controllers that condition pulse widths so that conventional phase detectors operate correctly. Lee takes only a single original input frequency from which Lee continually derives multiple frequencies at multiple outputs. Lee does not disclose or suggest any sort of composite phase-frequency detector.

Accordingly, withdrawal of this rejection is respectfully requested.

Claims 1-12 and 27-28 were rejected under 35 USC 101 for provisional double patenting in view of the claims of 09/653,788. It is noted that this divisional application was filed after the first restriction requirement in 09/653,788 and before the second reformulated restriction requirement in 09/653,788. Claims 1-12 and 27-28 are canceled without prejudice or disclaimer.

As noted above, pending claims 30-42 correspond to canceled claims 25-26 and 29 that were non-elected in the parent application. (Ser. No. 09/653,788). Pending claims 43-50 and 51-61 are also in accord with the restriction requirement set forth in the parent application because they do not require the feedback means delineated in the restriction requirement set forth in the parent application.

Accordingly, withdrawal of this rejection is respectfully requested.

Other than as explicitly set forth above, this reply does not include acquiescence to statements in the Office Action. In view of the above, all the claims are considered patentable

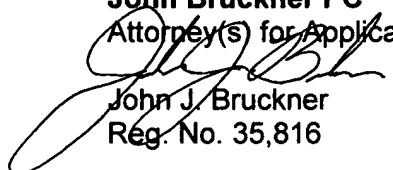
and allowance of all the claims is respectfully requested. The Examiner is invited to telephone the undersigned (at direct line 512-394-0118) for prompt action in the event any issues remain that prevent the allowance of any pending claims.

No fee is due for filing this Reply because it is being filed within the shortened statutory period for response as set in the Office Action dated August 18, 2004.

The Director of the U.S. Patent and Trademark Office is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-3204 of John Bruckner PC.

Respectfully submitted,

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Attorney(s) for Applicant(s)



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IN THE DRAWINGS:

Please substitute the attached Replacement Sheet(s) for its (their) corresponding drawing sheet(s) in this Application.

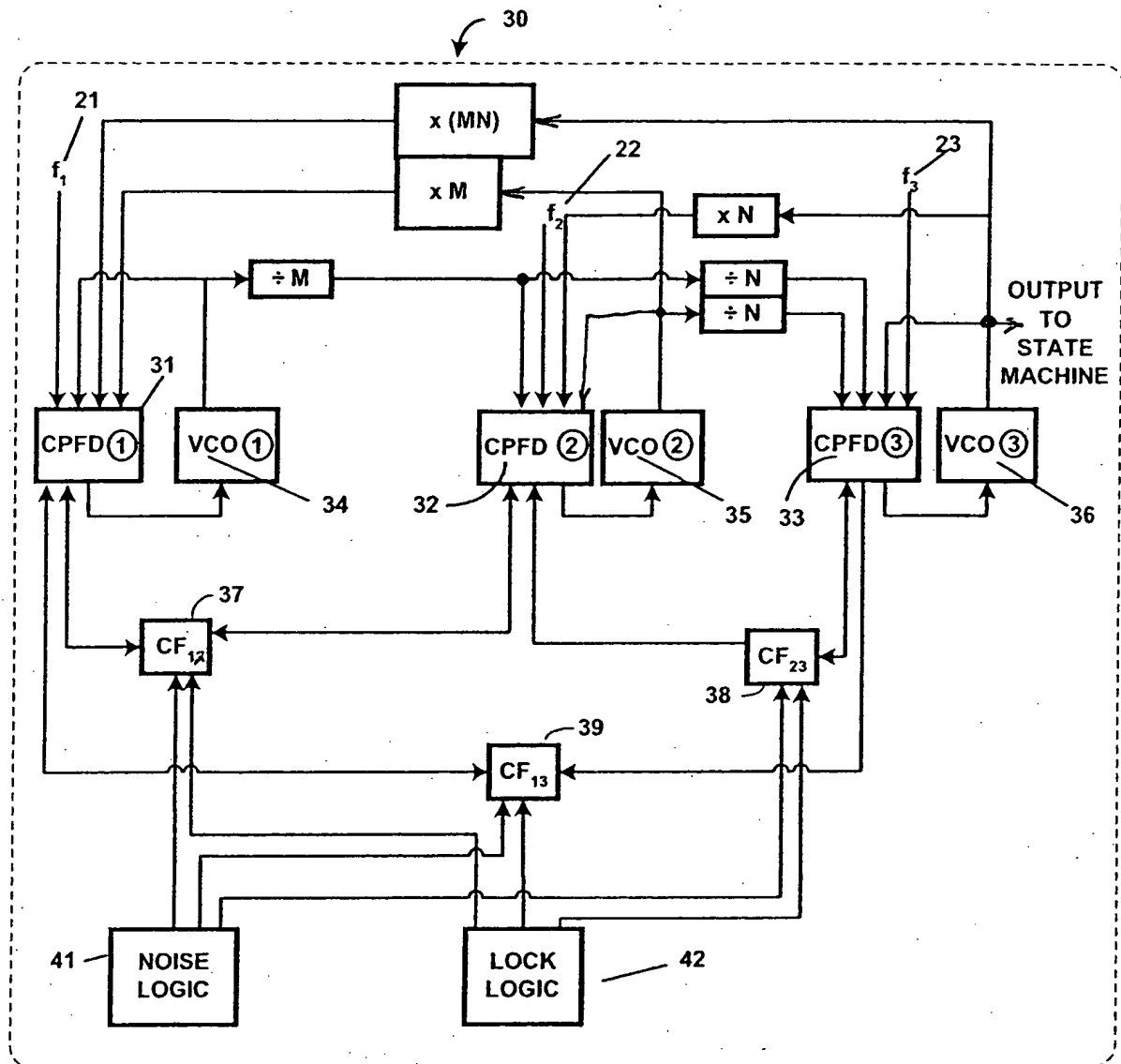


Fig. 3

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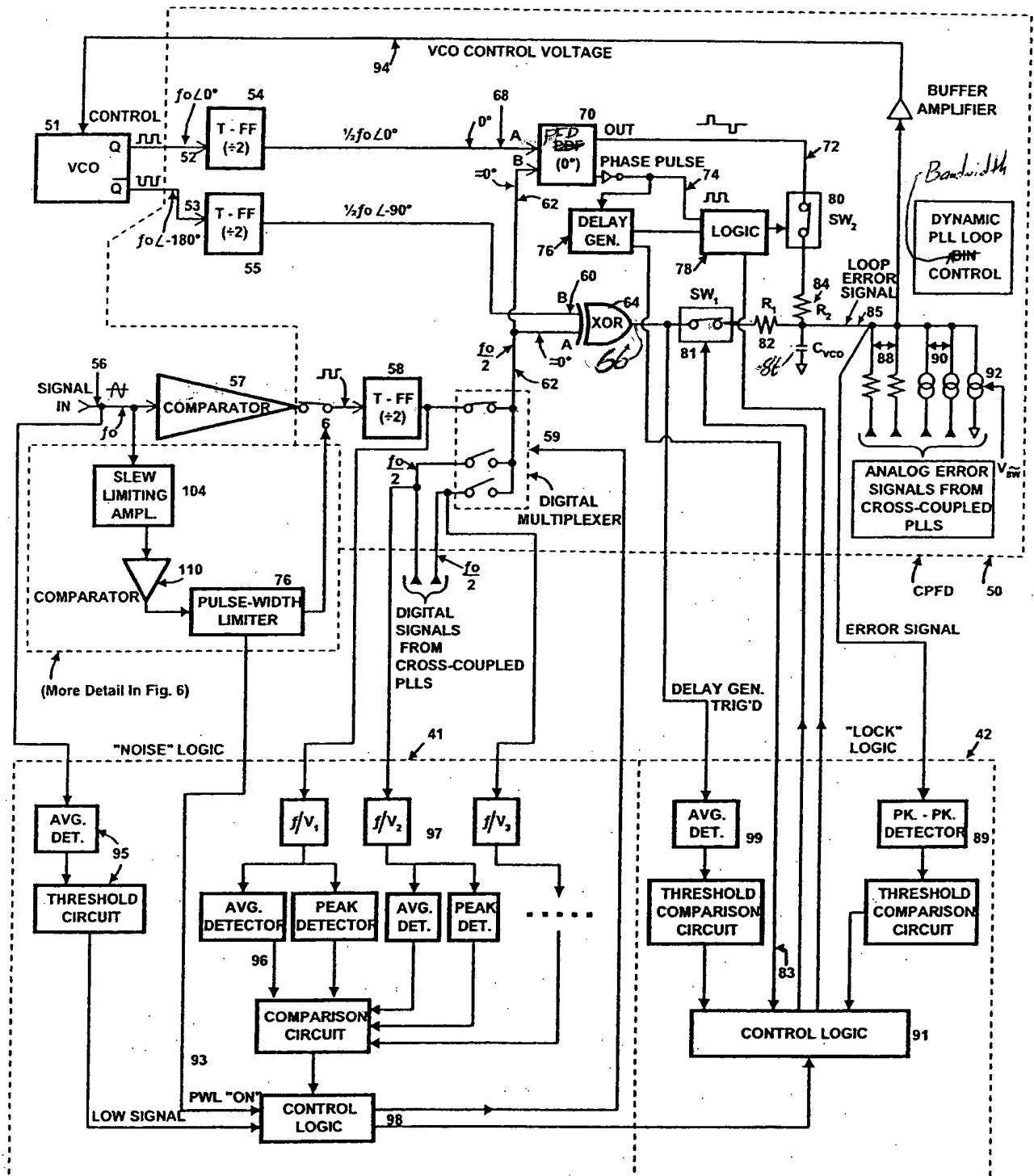


Fig. 5

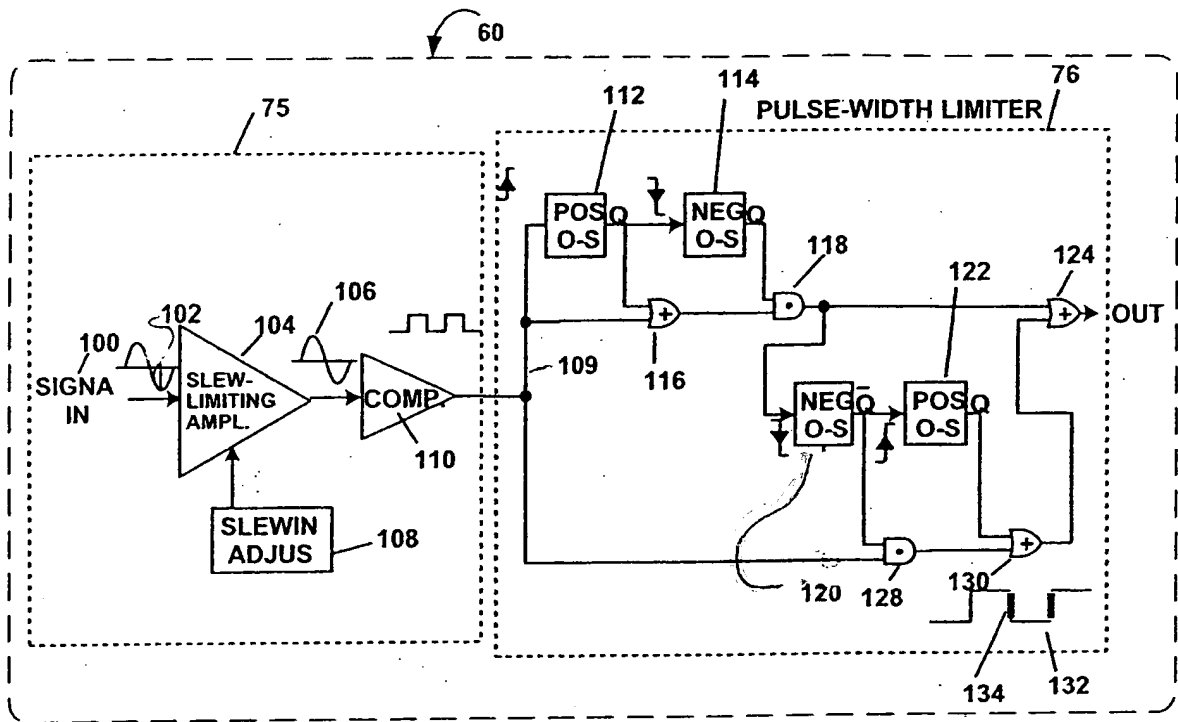


Fig. 6

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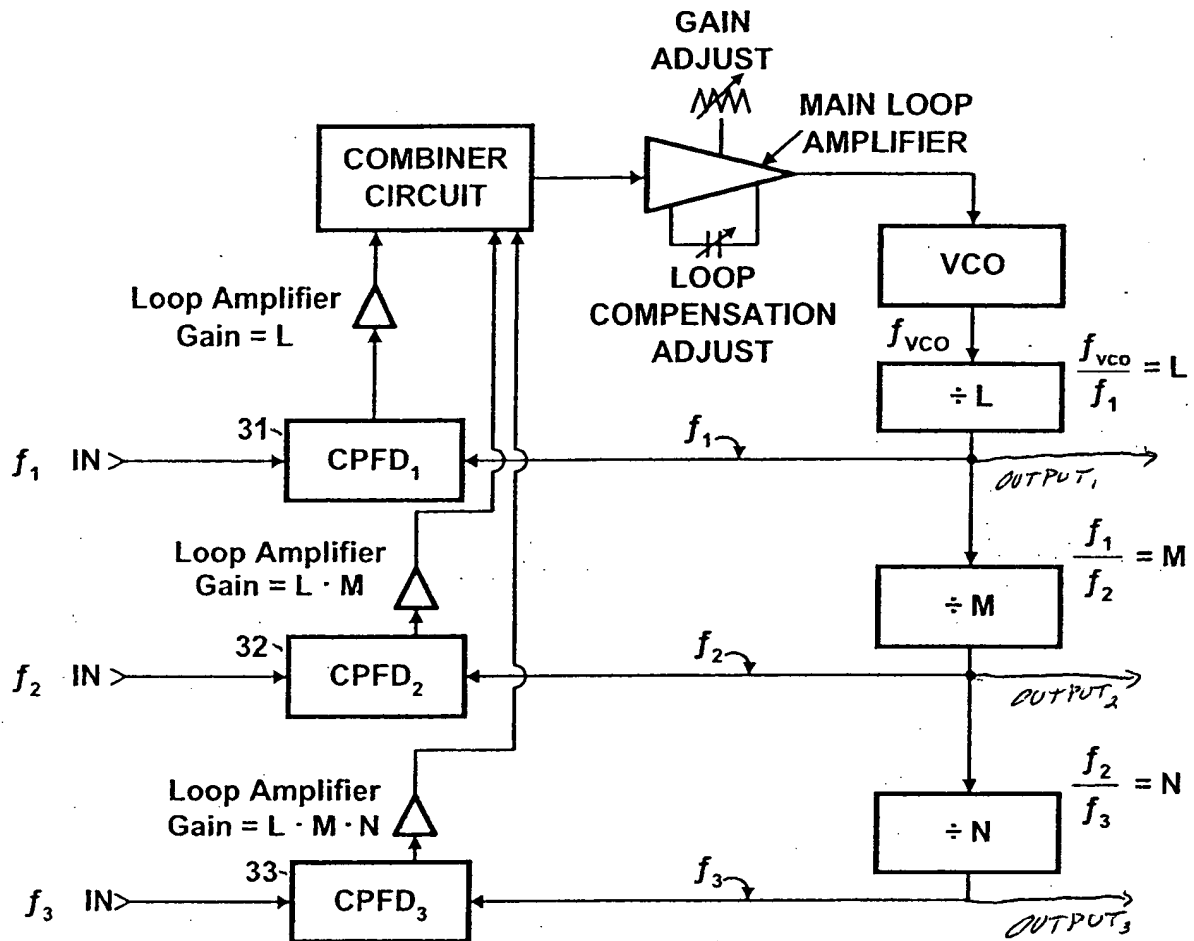


Fig. 7